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| 09/410,928      | 10/01/1999  | ANDREW M. JONES      | 99-TK-254           | 7656             |

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| EXAMINER |
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PEUGH, BRIAN R

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| ART UNIT | PAPER NUMBER |
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2187

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/410,928

Applicant(s)

JONES ET AL.

Examiner

Brian R. Peugh

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-16 and 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,7,9,10,13,15 and 19 is/are rejected.
- 7) ☒ Claim(s) 3,4,6,8,11,12,14,16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

This Office Action is in response to applicant's communication filed December 21, 2004, in response to Examiner's Action of September 23, 2004. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-16 and 19 have been presented for examination in this application. In response to Applicant's Amendment of December 21, 2004, claims 17 and 18 have been cancelled.

### ***Claim Objections***

Claim 6 is objected to because of the following informalities:

Regarding claim 6, line 5: Remove "main" in order to facilitate proper antecedent basis.

Regarding claim 6, lines 8-9: Replace both instances of "main memory" with --the memory system-- in order to facilitate proper antecedent basis [claim 5, line 3].

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, 10, 17, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Stamm (US# 5,432,918).

Regarding claim 1, Stamm teaches **a computer system comprising: a memory system where at least some of the memory is designated as shared memory** [memory (12); col. 4, lines 22-26]; **a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set** [Fig. 1; bus (11); col. 7, lines 43-48; CPU(10) inherently stores transaction that are to be 'initiated']; **a processor having a cache memory, the processor coupled to the memory system through the transaction based bus** [col. 3, lines 28-32; col. 4, lines 11-15; Fig. 1, backup cache (15) or primary cache (14)]; **a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components access the memory system directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus** [CPUs (28); Fig. 1; col. 4, lines 22-26]; **a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation** [data read; col. 7, lines 10-16], and

**wherein the processor is configured to respond to the request [data read] by treating the request as an explicit command to perform the cache coherency operation [data read, which necessitates the write-back to memory (12) operation to first be performed].**

Regarding claim 2, Stamm teaches **the request is implemented independent of any interrupt mechanism in the processor** [Stamm does not teach that an interrupt is necessary to implement the request, according to col. 7, lines 10-16].

Regarding claim 9, Stamm teaches **a method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules [system memory (12)]; modules refer to CPUs (10) & (28); Fig. 1; col. 4, lines 20-26], including a processing unit [CPUs (10) & (28)], and wherein the plurality of modules, including the processing unit, are coupled to a system bus [Fig. 1; col. 4, lines 20-25], the method comprising the steps of: causing the processing unit to cache at least some locations of the shared memory system in a cache memory [col. 3, lines 39-45]; initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation [col. 7, lines 10-16 & 43-48].**

Regarding claim 10, Stamm teaches **the step of initiating is performed without using an interrupt mechanism of the processing unit** [Stamm does not

teach that an interrupt is necessary to implement the request, according to col. 7, lines 10-16].

Regarding claim 19, Stamm teaches **the plurality of system components other than the processor are selected from the group consisting of: an external memory interface [col. 4, lines 20-22], a PCI bridge, peripheral subsystem interface, and direct memory access controller.**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 7, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stamm (US# 5,432, 918) as applied to claims 1, 2, 9, 10, 17, 18, and 19 above, and further in view of Farrall et al. (US# 2002/0007442).

Regarding claim 5, Stamm fails to teach that teaches the cache coherency transaction comprises a cache flush transaction and the request includes an address in the shared memory to be flushed from the cache. Farrall et al. teaches **the cache coherency transaction comprises a cache flush transaction and the request**

**includes an address in the shared memory to be flushed from the cache** [para. 82, 84 & 85].

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Stamm and Farrall et al. before him at the time the invention was made to modify the cache coherency system of Stamm to include the flush coherency mechanisms of Farrall et al., because then it is not necessary to request the cache coherency operation to be executed on a particular address stored in the cache, as taught by Farrall et al. [para. 18].

Regarding claim 7, Farrall et al. teaches **the cache coherency transaction comprises a cache purge transaction and the request includes an address in the shared memory to be purged from the cache** [para. 82 & 87-89].

Regarding claim 13, Farrall et al. teaches **the cache coherency transaction comprises a cache flush transaction and the step of initiating indicating an address in the shared memory to be flushed from the cache memory** [para. 82, 84 & 85].

Regarding claim 15, Farrall et al. teaches **the cache coherency transaction comprises a cache purge transaction and the step of initiating includes indicating an address in the shared memory to be purged from the cache memory** [para. 82 & 87-89].

***Allowable Subject Matter***

Claims 3, 4, 6, 8, 11, 12, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

Applicant's arguments filed December 21, 2004 have been fully considered but they are not persuasive.

Applicant argued on page 7, paragraph 3, that "Claim 1 calls for a system in which a request is defined by one of the plurality of system components and addressed to the processor where the request indicates an explicit request for the processor to perform a cache coherency operation. At least this feature of claim 1 is not shown or suggested in the relied on reference". The Examiner would like to point out that the claim recites that the request is actually issued, and not 'defined', by one of the plurality of system components. The Examiner would also like to point out that according to the claim language, the request is to be treated as an explicit command, not that the 'request indicates an explicit request'. The Applicant then proceeds to describe the Stamm reference and indicates that "...Table B lists these "cache coherency commands". In fact, these commands appear to be read and write commands that implicitly indicate that the CPU should perform a cache operation rather than an explicit command to perform a particular cache coherency operation. As noted in the Stamm



reference at column 7, lines 52-54, a cache coherency command will not necessarily cause a CPU to perform any cache operation. Hence, the commands listed in Table B are not treated as an explicit instruction to perform a cache coherency operation as called for in claim 1.” The Examiner disagrees with Applicant’s assessment, because according to col. 7, lines 52-54, the cache coherency command will occur if the cache block is owned by another CPU. If the cache block is owned by another CPU, a writeback coherency operation will then ‘explicitly’ occur due to these specific circumstances surrounding the IREAD command, for example, as found in Table B. Table A also illustrates the cache coherency operations necessary to be taken in response to cache block operations.

Regarding Applicant’s argument of Claim 9 in that “... the rejection stated in the Office Action does not point to any portion of the Stamm reference that shows a component other than a CPU initiating a cache coherency transaction.” The Examiner would like to point out that ‘another CPU’ fulfills the claim requirement of “one of the plurality of modules other than the processing unit” found in claim 9 and recited in the Examiner’s Office Action on page 6, line 2.

Regarding Applicant’s arguments regarding the 35 U.S.C. 103 rejection, in that the Farrall reference does not supply the deficiencies of Stamm, the Examiner has illustrated above that Stamm teaches all of the claim limitations and thus the 35 U.S.C. rejection is proper.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

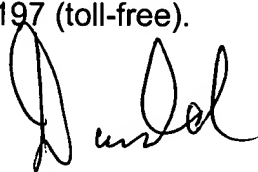
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian R. Peugh  
Patent Examiner  
Art Unit 2187  
February 28, 2005



DONALD SPARKS  
SUPERVISORY PATENT EXAMINER